Summary of TEMIC Visit and FE-D Issues

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Overview of our visit to TEMIC:

- Topics of discussion
- What was learned

Summary of known Problems and Issues with FE-D:

- Analog
- Integration
- Digital Readout

Next steps with FE-D and preparation for FE-D2 submission:

- Study bump-bonded assemblies from Alenia and IZM
- Backup wafer run with TEMIC

Issue List for TEMIC Visit

Fabrication problems with FE-D run:

- Low shift register yield and “leaky PMOS” analysis
- Digital Readout “row 0” problem and “leaky NMOS” analysis
- Anomalous DC digital power consumption

Yield issues

- Advice DRC rules, other guidance for improved yield, expected/minimum yield

Process issues

- Voltage limits: transient and operating voltages

Standard Cell Library issues

- Post-rad simulation models, support for back-annotation of loads and power consumption estimates

Design kit issues

- Fix of bugs (VTCAPA check, I/O pad stream-out) and support for HSPICE
- Improved DRC checking support (DRACULA)

Process monitoring strategy

Process Monitoring Strategy

PCM (process control monitor) in dicing streets:

- Presently monitor 90 parameters, of which 30 are “critical” or “reject” parameters (typical large-volume process, monitor 30 of which 10 are reject).
- All parameters are recorded for 5 die sites per wafer (a total of 60 sites exist on each wafer). Reject parameters must lie within control limit windows for 3 of these 5 sites for wafer acceptance.
- Parameters values used to “tune” line using statistical process control to progressively force parameter values to center of limit windows with small variation. New reject parameters can be added, and windows adjusted to optimize yields.

Radiation qualification:

- Test two die sites on a wafer at 10 MRad using X-rays, one of which must pass limit windows for acceptance. Either parameters are guaranteed (g_m, V_T, ID, β). Presently re-writing qualification specs, but will either irradiate 1 or 2 wafers per lot. Presently do not monitor prerad values of parameters for these wafers (will be added).
- We have requested that we be able to receive all of this data electronically for each lot throughout engineering and production runs. TEMIC not enthusiastic, but we argued “we are scientists and like data”.

Yield Issues

- Lengthy discussions of yield and expectations. Data shown for other higher volume processes, to indicate how the production matures and the yield improves with volume. DMILL is not likely to ever reach the later stages of this learning curve...
- Standard yield model depends on D (defect density), A (area), and C (complexity), and has approximate form: yield = $1/(1+ACD)^n$, where n is typically 1-2. For 80mm^2 pixel die, target yield is about 35%, with minimum yield about 20% (approximate numbers from CERN Frame contract).
- Claim, given recent experience with yield for smaller die, we should be getting about 15-25% yield for pixel FE chip today. We need formula to evaluate complexity, and bipolar yield may be lower.
- First stage of optimization involves running several lots per month, which typically allows reaching about 80% of the target yield, which would produce a pixel chip yield of about 27%, and would imply about 1500 wafers needed for outer layers.
- However, all of this discussion was quite “fuzzy”, and will be design dependent.
- Most mature HEP example is ABCD. For 40 mm^2 digital design area, acheive a 40-45% yield, which is roughly 80% of the target value. Analog section yield, which is dominantly bipolar, is much worse: about 60% for 7mm^2.

Process Issues

Series of limiting voltages which can cause rapid device failure:

- Breakdown (serious damage normally follows without careful current limiting): NMOS is lower than PMOS.
- NMOS spec is >8.0V in off-state. Note in general for CMOS, devices in on-state have much less than the supply voltage across their terminals, in contrast to those in the off-state. The off-state breakdown voltages are monitored (BVN08, BVP08), and are typically 11-12V for both NMOS and PMOS. The on-state voltage is not monitored, and is about 6.5V for the worst case Vg of 2.5V.
- Bipolar breakdown (BVCEO, max voltage between collector and emitter) is 5.5V (previously 5.7V).
- Careful study of circuits needed to translate these limits into power supply limits.

There are two major lifetime issues:

- Time dependent oxide breakdown can occur with a gate oxide field above about 4MV/cm, corresponding to about 7V on the gate. This can cause problems over 10 year periods.
- Hot carrier effects injecting electrons into gate oxide and shifting gm and Isat, limit maximum continuous supply voltage to less than 5.5V for 10 year lifetime.

Standard Cell and Design Kit Issues

Standard Cell Library:

- Maintenance taken over by TEMIC from IMEC. No immediate upgrade plans, but plan to re-characterize the library.
- Have been requested to re-characterize and provide corner models (particularly post-rad). They promise to investigate the required effort.
- Have capability to do back-annotation for other processes using Cadence TLF (Timing Library Format) format which allows creating SDF files for Verilog simulations, and propose to provide this in 2/2000 for DMILL. This new version of the libary will also be compatible with Cadence 4.4.x
- Have tool for power consumption simulations for other processes, TEMIC will investigate conversion effort required for DMILL.

Design Kit:

- Kit being updated to V5.1 after several bug fixes, including VTCAPA problem of FE-D, missing rule for GENRES layout, and missing stream-out of I/O pad info.
- Claim their comparisons of HSPICE and ELDO for TEMIC BSIM3 models showed good agreement. Suggested that this is only true for recent versions of HSPICE.
- Request for support for better DRC tool (beyond DIVA). TEMIC presently uses CALIBER instead of DRACULA, and could consider supporting CALIBER rule

Specific FE-D Issues

Low yield for Pixel Shift Register

- After careful analysis by Bonn, presented to TEMIC in detail, we are convinced there are fabrication problems in small number of min-size PMOS in SR.

Problems in Pixel Digital Readout

- Very complex problem, lots of analysis from Bonn and LBL. Strong correlations between excessive current associated with certain pixels and readout and “row 0” problems with these same pixels. We are convinced there are fabrication problems with min-size NMOS in dynamic block in pixel hit logic.

Anomalies in Digital Power Consumption

- Many chips show anomalous excess DC consumption on VDD, which we believe must also be associated with fabrication defects.

Observation:

- Do not see failures in other sensitive circuits with more devices (PMOS in Cal inject and in LE/TE RAM), and do not presently understand why this is the case.

Additional observation:

- LArg group observed a low yield for most recent (third) version of their SCA chip. Observed fault is leaky cells, with equivalent MOS resistance of 1-10 gigohm.

Proposed FE-D Actions

- High/Low T characterization of “leaky” NMOS/PMOS problems to check whether there is a significant dependence or not (Bonn+LBL).
- Physical analysis of some defective samples by TEMIC: “reverse engineer” chips in region of bad transistors, removing one layer at a time and looking for fabrication faults (Bonn to send devices to TEMIC).
- Use FIB surgery to add small probe points to defective transistors to try to observe behavior and confirm defect theory - may require better probes (LBL).
- Discuss details of layout in defective areas with LETI experts to see if there are any special issues there which are not known to TEMIC (Bonn+CPPM).
- Processing of four backup wafers (presently awaiting poly patterning). TEMIC will advise us on whether they consider it useful to modify the poly gate sizes (“run poly corners”). TEMIC investigating foundry schedule, but could be only 4-6 weeks to process. We propose minor changes in the M1 and M2 masks:

  Make small windows in M2 over the critical dynamic nodes in the Pixel Register and the digital readout cell to allow non-invasive diagnostics (e-beam or thermo-luminessence).

  Investigate moving vias over critical transistors (allowed by DRC, but suspicious).

  Cut VTH amplifier connection, and make GA2 connection.

  Investigate possibility of “patching” a non-critical buffer between SDO and Output MUX.

- Want to modify one die in reticle and leave the other alone for control of new run.

Known Problems and Issues with FE-D

Analog Section:

- Fix for VTH Amplifier to eliminate shorts between filtering capacitors
- Large threshold dispersion observed at low VCCD/VTH
- Large threshold sensitivity to small changes in VCCD/VTH for large VCCD/VTH. Also re-examine range of VCCD/VTH DACs to optimize step size.
- Systematic variations in threshold, noise, and TOT observed within FE-D chips
- Preamp risetime and front-end timewalk performance under realistic C(load)
- Instability in operation of front-end after Hard Reset
- Minor improvements in Chopper design

Integration:

- Digital supply consumption is too high (fabrication problems ?).
- Buffer size problems in command decoder for Load_Mask, Load_Bit0/1/2, and Load_Reg signals.
- Buffer size problems for CLK1/CLK2 (maybe require distributed buffering).
- Buffer size problems in XCK distribution.
- Insert buffer at serializer output (SDO).
- Check for proper buffering between all circuit blocks.
- Re-examine all buffer sizes, particularly post-rad, to make sure adequate margin exists. Most likely, examine all nodes in design with loads above about 200fF.
- Fix missing connection to GA2 pad

Digital Readout:

- Add masking of Buffer Overflow into column mask block.
- Study “row 0” problem further to make sure there are no design errors contributing to the strange observed behavior.
- Investigate further the sensitivity of data readout to sense amplifier bias.
- Verify buffering in bottom of chip by doing ELDO simulations with netlists extracted from layout (full annotation of parasitic capacitances).

Minor Upgrades:

- Add control bit to Chopper to allow monitoring low scale from off-chip.
- Improve Self-Trigger circuit to operate as intended in final chips (Enable trigger in Global Register, but require actual LVL1 to activate trigger)
- Investigate improving synchronization information in EOE word (send LE timestamp = BCID), and improve ability to synchronize timestamp generator (SoftReset)

Next Steps for FE-D

- Work on list of action items, mainly trying to measure MOS defects using FIB modifications to prove they are not design faults.
- Continue characterizations to see if there is some “fine-tuning” of analog section to do, and to try to understand lack of stability in analog performance with reset.
- Characterize bump-bonded assemblies as soon as they return (may require additional surgery on some to make SDO mod to allow 3.0V VDD operation).
- Work on modifications for backup wafer run. The M1 and M2 masks are not needed immediately (only poly is critical, since it is next processing step). This run may take some time to return, and we may not wait for these wafers before sending in FE-D2.
- Complete presently known modifications to FE-D design database to make FE-D2. List of changes is quite modest (but critical !).
- Continue intensive simulation and verification work on FE-D2 database.
- Do PS irradiations on PM bars and Analog Test chips to validate performance of individual devices and analog portions of FE-D under irradiation.
- Actual submission date for FE-D2 will depend on factors above, but should be as early as possible (March) to allow us to complete serious evaluation this Summer (PS and other irradiations, single-chip and module assemblies, testbeams, etc.). Several activities above may not be completed by submission date.

Proposed reticle would include:

- Two FE-D as now,
- Revised Analog Test chip (include prototype of Strobe Delay block for MCC ?)
- PM bar plus TEMIC PM structures
- LVDS Buffer chip
- Revised DORIC and VDC (depending on their status)
- Remove MCC-D0, as no more are needed and it is large
- Re-adjust reticle layout to fix minor problems from the previous run (dicing streets and reticle orientation to minimize losses in exclusion region).